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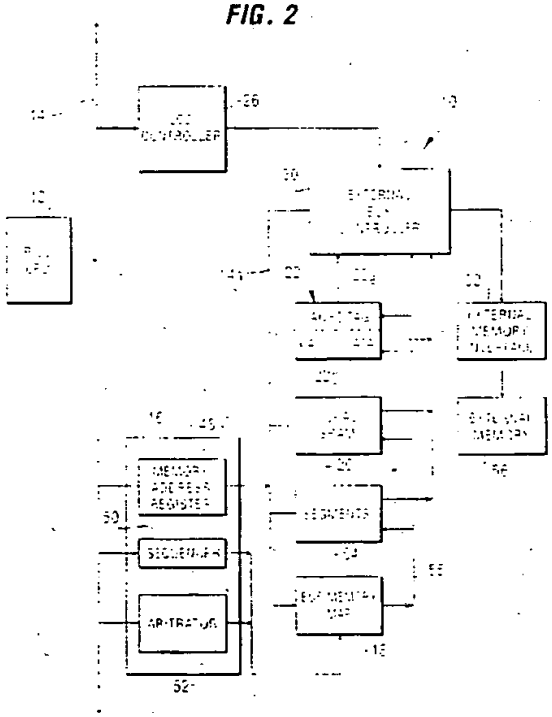
(54) Memory protection mechanism

(57) A memory protection mechanism provides for the segmenting of memory addresses, which allows for a larger addressable memory space than would otherwise be expected from the 26-bit external address bus of the integrated circuit. Up to eight segments of memory may be defined, each of which may be programmed for start and stop addresses, access privileges, cacheabilty, memory word-length criteria, and memory bank assignment. Because multiple segments are associated with the chip enable, a single physical memory block may be divided into user and supervisor segments for both data and program memory. Such an arrangement provides additional memory segments over the conventional enable structure, and allow for separation of memory blocks without sacrificing other control capabilities.

FIG. 2



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ory blocks without sacrificing other control capabilities

These and other objects and advantages of the invention will become more fully apparent as the description which follows is read in connection with the drawings.

Brief Description of the Drawings

Fig. 1 is block diagram of the system on chip structure of the invention.

Fig. 2 is a detailed block diagram/flow chart of a portion of the system on chip structure of Fig. 1.

Fig. 3 is a block diagram of the segmented memory structure of the invention.

Fig. 4 is a block diagram of a segment descriptor register of the invention.

Best Mode of Practicing the Invention

Referring initially to Fig. 1, a system on chip (SOC) structure of the invention is depicted generally at 10. IC 10 includes a RISC CPU 12 which is connected to a 32-bit internal bus 14. CPU 12 includes an embedded microcontroller 12a therein in the preferred embodiment CPU 12 is directly connected to internal bus controller 16, which in turn is connected to bus 14 and to a bus, or memory, map 18. IC 10 further includes a local RAM (SRAM) 20, a combined instruction/data cache 22, and an external access port 24. In the preferred embodiment, IC 10 is intended to connect to a liquid crystal display (LCD) and to that end, includes a LCD controller 26 which is connected to an LCD panel interface 28. An external bus controller 30 is provided and is connected to an external memory interface 32 and external chip selects 34, which may be constructed as part of the external bus controller.

A number of configuration registers 36 are provided, which may be constructed as a part of internal bus controller 16. A number of internal "peripherals" are connected to internal bus 14 and include a universal asynchronous receiver/transmitter (UART) 38, a parallel port 40, a timer/counter 42, an interrupt controller 44 and a pulse width modulator (PWM) 46

Referring now to Fig. 2, a portion of IC 10 is depicted. For purposes of this description, internal bus controller 16 is shown in more detail, and includes a memory address register 48, a sequencer 50, and an arbitrator 52. The internal bus is depicted in two segments, 14 and 14a. Memory address register 48 receives and stores a memory address from CPU 12 and attempts to locate that address in the various on-chip internal memory structures, such as cache 22, which is split into a cache Tag portion 22a, and a cache data portion 22b, local SRAM 20, memory map 18, or memory segments 54. The address is also passed to sequencer 50 and arbitrator 52 which determine whether the address is a sequential address from the previous memory address request (sequencer 50) and whether there are other operations that take priority over the present search on a particular clock cycle (arbitrator 52). In the case where the memory address is sequential with the immediately prior request, a signal is passed to memory map 18 which sends an abort signal 55 to the internal memory structures, with the exception of the structure that contains the next sequential address. In the event that the address is not found in any of the internal memory structures, external bus controller 30 will initiate a search for the address in external memory 56

Referring now to Fig. 3, plural memory segments 54 are depicted in greater detail, along with selected associated structures. In the preferred embodiment, there are eight memory segments, segments 0-7, shown generally at 58. Each segment includes three registers: A segment descriptor register (SDR) 60, a start register 62, and a stop register 64. A separate default SDR 66 is provided and is used after reset or, if-and-only-if (iff), in the event a search for the memory address is not found in SDRs 0-7. Memory segments 54 provide the addresses of multiple memory regions which are to be mapped to the same physical memory structures locations, either local RAM 20 or external memory 56. RAM 20 and external memory 56 both contain multiple memory regions located in a single physical location. A memory region, or memory bank, may be defined in a physical memory structure by setting a starting memory address in one of the start registers 62 and by setting an ending memory address in one of the stop registers 64.

Each SDR contains information about address characteristics, including system privileges, user privileges, cacheability, word length characteristics, and memory bank selection. Each segment may map to only one memory bank, represented generally by block 68, which is located in external memory 56. Start register 62 and stop register 64 determine the boundaries within memory of each segment. Each start and stop register is a 32-bit register, and contains a start or stop address of 22-bits, in bit locations 10-31. Bits 0 - 9 are zero-filled and are used to convert a 22-bit address to a 32-bit address. Default SDR 66 does not have start/stop registers associate therewith, as the default SDR spans the entire memory bank space. All of the start/stop registers will initialize to a zero-fill upon reset, forcing any external memory access to the default segment

Embedded microcontroller 12a supports eight memory banks, six of which are for SRAM functions and two of which are for DRAM functions. A SRAM bank will reflect the properties of an external SRAM, such as chip selects, wait counts, and bus width. A DRAM bank will reflect the properties of an external DRAM such as nCAS (not Column Address Select), nRAS (not Row Address Select), memory bank size, page mode, wait count, and bus width

When external bus controller 30 receives an internal address for memory access from memory address register 48, it maps the address to the appropriate segment, or to the default segment, and performs all the

receipt of a memory address from said address register. compares the memory address to the multiple memory regions to locate the physical memory location.

2. The memory protection mechanism of claim 1 wherein said plural memory segments each include a segment descriptor register for setting said address characteristics. a start register for receiving the starting address of a physical memory block. and a stop register for setting the ending address of a physical memory block

3. The memory protection mechanism of claim 2 wherein said segment descriptor register includes plural characteristic blocks associated with the address characteristics. including a system privilege block. a user privileges block. a chacheability block. a word-length block. and a memory bank assignment block.

4. The memory protection mechanism of claim 2 which includes a default segment descriptor register which is used after a system reset and iff a memory address does not match an address in any other segment descriptor register.

5. In an integrated circuit having a RISC CPU. a memory management module and on-chip. internal memory structures. and connected to an off-chip. external memory structure. an on-chip memory protection mechanism for enhancing addressable memory space while prohibiting the overwriting of privileged memory contents. comprising:

a memory map structure for mapping memory addresses of memory contents in the internal memory structures and in the external memory structure:
address characteristic associated with each memory address.
a memory address register for reciving and storing a memory address from the CPU. and
plural memory segments. each including each include a segment descriptor register for receiving said address characteristics. a start register for setting the starting address of a physical memory block. and a stop register for setting the ending address of a physical memory block. for providing the addresses of multiple memory regions to be mapped to the same physical memory structure location. wherein said multiple memory regions contain different memory contents having predetermined privileges. and for receiving information about said address characteristics. and wherein said plural memory segments. upon receipt of a memory address from said address register compares the memory address to the multiple memory regions to locate the physical memory location.

6. The memory protection mechanism of claim 5 wherein said segment descriptor register includes plural characterisic blocks associated with the address characteristics. including a system privilege block. a user privileges block. a chacheability block. a word-length block. and a memory bank assignment block

7. The memory protection mechanism of claim 5 which includes a default segment descriptor register which is used after a system reset and iff a memory address does not match an address in any other segment descriptor register.

8. An integrated circuit (10) connectable to an off-chip. external memory structure (56). and having a RISC CPU. a memory management module on-chip. internal memory structures (20). and an on-chip memory protection mechanism for enhancing addressable memory space while prohibiting the overwriting of privileged memory contents. said memory protection mechanism comprising:

a memory map structure (30) for mapping memory addresses of memory contents in the internal memory structures (20) and in the external memory structure (56):
a memory address register (48) for receiving and storing a memory address from the CPU: and
plural memory segments (54) for providing the addresses of multiple memory regions to be mapped to the same physical memory structure location wherein said multiple memory regions contain different memory contents having predetermined privileges. and for receiving information about said address characteristics. and wherein said plural memory segments. upon receipt of a memory address from said address register (48). compares the memory address to the multiple memory regions to locate the physical memory location.

9. An integrated circuit having a RISC CPU and an on-chip memory protection mechanism for enhancing addressable memory space while prohibiting the overwriting of privileged memory contents comprising.

a memory map structure (30) for mapping memory addresses:
a memory address register (48) for receiving and storing a memory address from the CPU: and

FIG.1

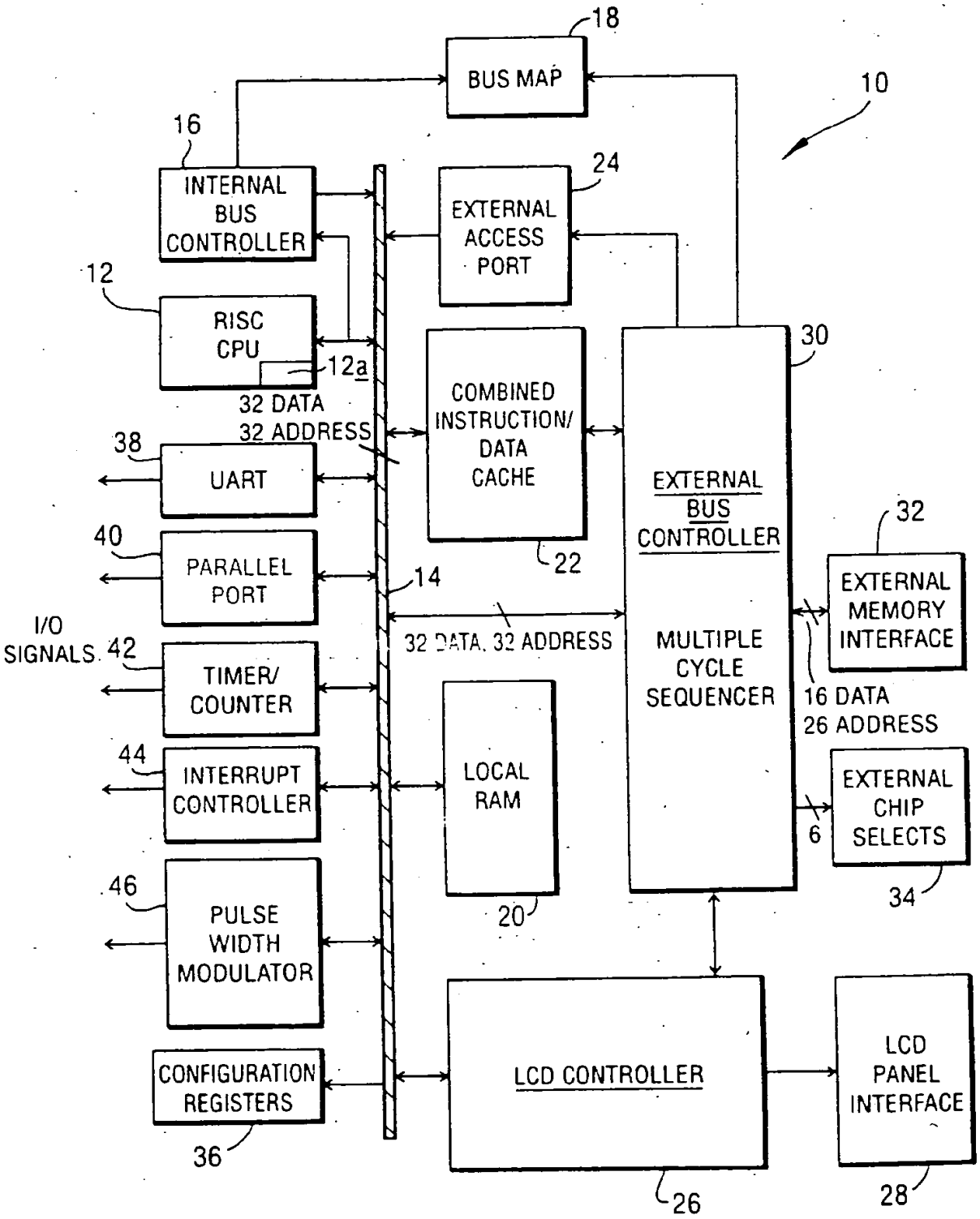

18
BUS MAP
10
16
INTERNAL BUS CONTROLLER
24
EXTERNAL ACCESS PORT
12
RISC CPU
12a
32 DATA
32 ADDRESS
COMBINED INSTRUCTION/ DATA CACHE
22
30
EXTERNAL BUS CONTROLLER
MULTIPLE CYCLE SEQUENCER
38
UART
40
PARALLEL PORT
14
32 DATA, 32 ADDRESS
I/O SIGNALS
42
TIMER/ COUNTER
44
INTERRUPT CONTROLLER
LOCAL RAM
20
32
EXTERNAL MEMORY INTERFACE
16 DATA
26 ADDRESS
EXTERNAL CHIP SELECTS
6
34
46
PULSE WIDTH MODULATOR
CONFIGURATION REGISTERS
36
LCD CONTROLLER
26
LCD PANEL INTERFACE
28

FIG.3

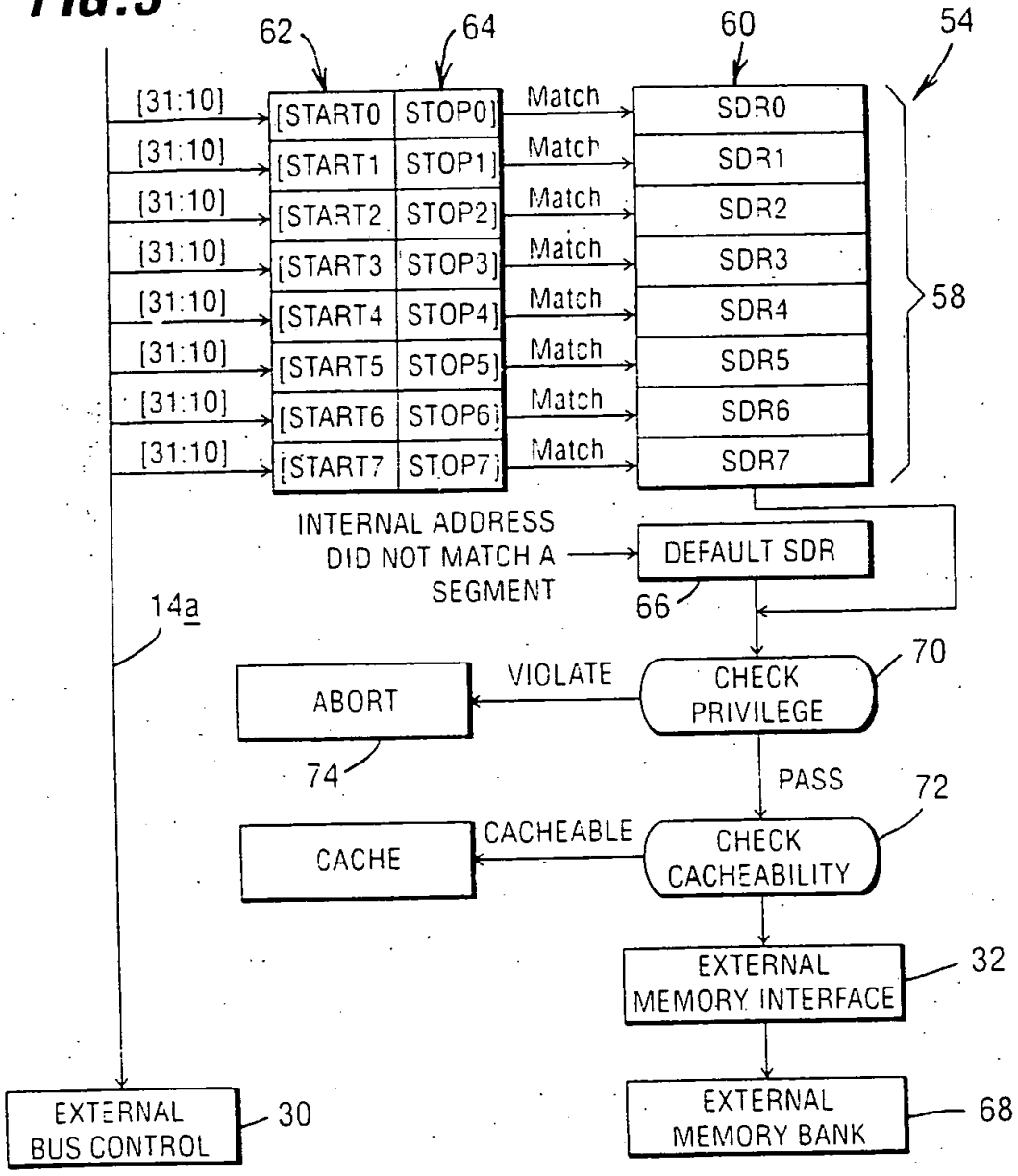
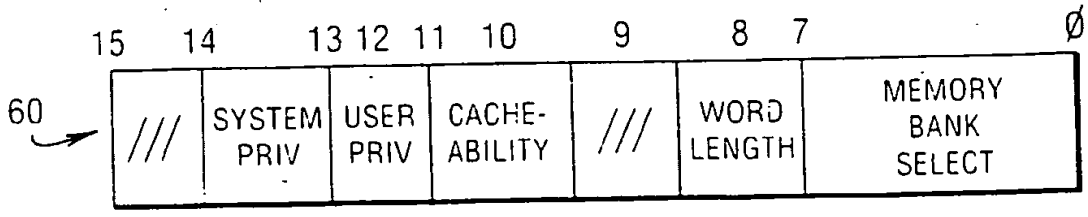

62
64
60
54
[31:10]
[START0 STOP0]
Match
SDR0
[START1 STOP1]
SDR1
[START2 STOP2]
SDR2
[START3 STOP3]
SDR3
[START4 STOP4]
SDR4
[START5 STOP5]
SDR5
[START6 STOP6]
SDR6
[START7 STOP7]
SDR7
58
INTERNAL ADDRESS DID NOT MATCH A SEGMENT
DEFAULT SDR
66
14a
ABORT
VIOLATE
CHECK PRIVILEGE
70
74
PASS
72
CACHE
CACHEABLE
CHECK CACHEABILITY
EXTERNAL MEMORY INTERFACE
32
EXTERNAL BUS CONTROL
30
EXTERNAL MEMORY BANK
68

FIG.4


15
14
13 12
11
10
9
8
7
Ø
60
///
SYSTEM PRIV
USER PRIV
CACHE-ABILITY
///
WORD LENGTH
MEMORY BANK SELECT

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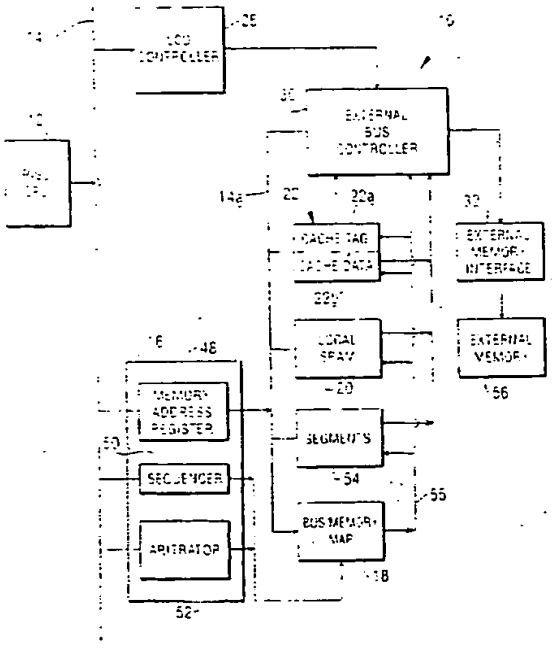

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EUROPEAN SEARCH REPORT

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	COMPUTER, vol. 20, no. 3, March 1987, NEW YORK US, pages 48-67, XP002034222 FURHT B ET AL: "A SURVEY OF MICROPROCESSOR ARCHITECTURES FOR MEMORY MANAGEMENT" * page 52, column 3, line 57 - page 53, line 55 * * page 58, column 1, line 4 - column 2, line 12 * * page 64, column 2, line 9 - column 3, line 37 * * figures 8-10,27 * -----	1,5,8,9	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	2 July 1997	Masche, C

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